

Ultra Low-Latency 25Gbit/s Ethernet PCS

CT1026-25GPCS - Product Brief - Version 1.1 – 6th July 2017



The Chevin Technology 25GPCS provides Ultra low-latency 25Gbit/s Ethernet connectivity in Xilinx Virtex® Ultra Scale™ FPGAs. Ultra-low latency is achieved by using only the PMA function in FPGA Multi-Gigabit transceivers, and moving all PCS functions to code that is optimized for 25GBASE-R. This allows the data to take the shortest and lowest latency path, to and from the wire.

The 25GPCS /PMA core can be used directly with Multi-Gigabit Transceivers (SerDes & CDR logic) in Xilinx Virtex® UltraScale FPGAs for the lowest possible latency. The application side can be driven by any 25GMII compatible MAC with a 64bit interface at 390.625MHz, however we recommend using our 25GMAC for ease of integration and minimal latency.

The PCS manages link encoding and scrambling, while adapting the data rate to the reference clocks. A detailed statistics block provides a running count of frames sent and received with individual 64bit counters for frames, BER events, illegal codes and decode errors, which can be monitored through the Host Interface.

Achieve speedy, straightforward integration with the reference design on Alpha Data's ADM-PCIE-8V3 board, using standard software development tools, when integrated with higher layers from Chevin Technology's portfolio of IP cores. The 25GPCS is also suitable for Xilinx's VCU108 board.

Key Features

- Designed to IEEE 802.3by
- Low Latency PCS/PMA (RTT) 99 ns
- 5250 LUTs
- Integrated 64b66b encoder/decoder
- Integrated Scrambler/Descrambler
- Gearbox for rate conversion
- Fault management, BER monitoring
- Clock Rate adaptation, TX/ RX
- Detailed traffic analysis statistics collection
- XXVGMII interface, 64bit @ 390.625MHz
- Connect directly using SFP28
- Use 4-channel for QSFP28 interfaces

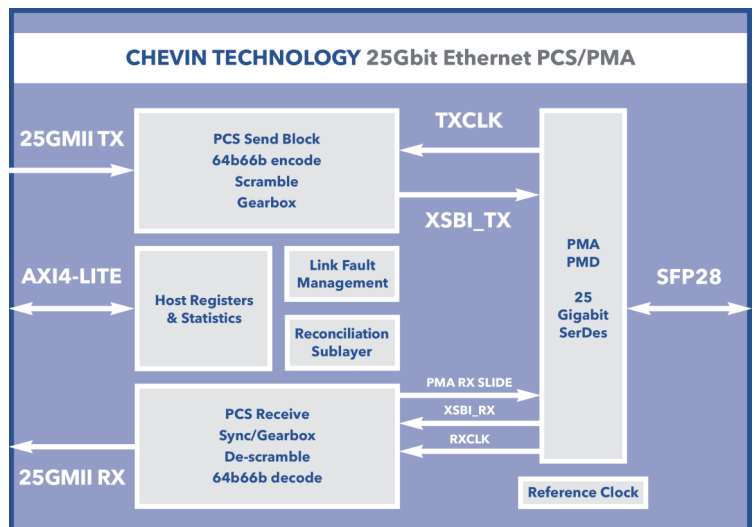
Latency Figures

Round trip delay, PCS/PMA
25GMII -> SFP28 (wire) -> XGMII 99ns

Combined MAC & PCS/PMA
Round trip delay (Ultrascale)
MAC(in) -> SFP28 (wire) -> MAC(out) 120ns

FPGA Resource Figures

Device: Virtex® UltraScale™ xcvu095 -2
PCS/PMA 5250 LUTs



Deliverables

- Encrypted RTL/VHDL source code for simulation
- Encrypted compiled netlist
- Datasheet & User Guide to assist integration
- Reference Designs for Alpha-Data boards
ADM-PCIE-KU3, ADM-PCIE-8V3, ADM-PCIE-9V3
- Simulation Test bench
- Build scripts for Vivado/ISE
- Support for integration into FPGA



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25Gbit/s Ethernet PCS

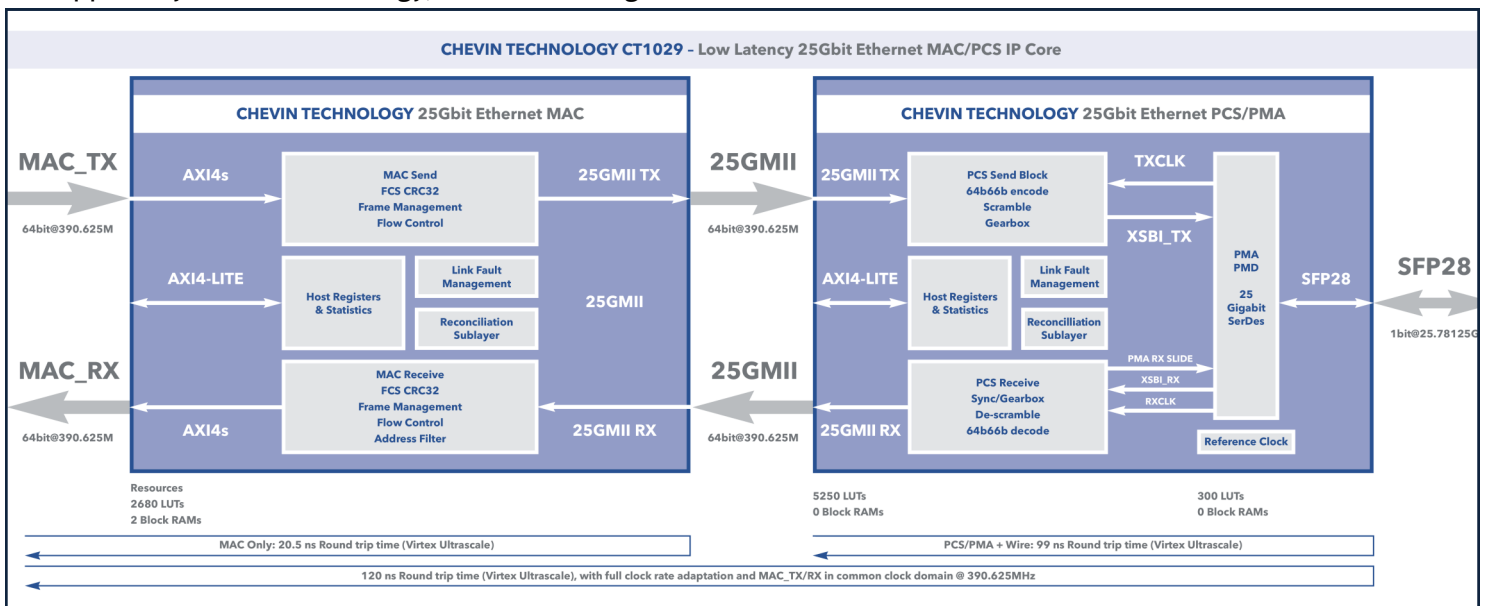
25GPCS - Integration in FPGA

Integration is made simple with the reference design, which includes the MAC function and a block for UDP/ICMP/ARP. A simple UDP based host interface allows control and configuration of the 25GPCS registers and statistics block. The reference design documentation describes how to add constraints and build a 4-channel PCS block into your application.

The Xilinx UltraScale™ Multi Gigabit Transceivers combined with a compact soft PCS provides the lowest possible latency at 25Gbit/s; ideal for challenging applications that require combined low latency and high performance.

Reference clock: 161.1328125 MHz

The application side connects directly to any 25GMII compatible MAC, however we recommend pairing the 25GPCS with Chevin Technology's 25GMAC and other stack layers such as TCP/IP, UDP/IP, ICMP and ARP, also supplied by Chevin Technology, for a more integrated FPGA solution.



Chevin Technology IP



10G MAC

10G LL MAC & PCS/PMA

10G PCS/PMA



SATAv3.2 – 1.5/3/6Gbit/s
SSD Host Ctrl



25G MAC

25G PCS/PMA

25G LLMAC & PCS/PMA



25G UDP, 25G TCP

10GTCP - 10Gbit/s TCP Server/Client
10GUDP - 10Gbit/s UDP Server/Client
10GICMP/ARP – 10Gbit/s support library
10GUDT4 – 10Gbit/s UDT4 Server

Markets

- Finance
- Telecoms
- Broadcast
- Defense/ Government
- Oil and Gas

Applications

- Trade execution & monitoring
- Data Storage & Capture systems
- HPC / Big Data systems
- Signal processing systems
- Data Mining

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