

Ultra Low-Latency 10Gbit/s Ethernet MAC

CT1009-XGMAC - Product Brief - Version 1.8 – 6th June 2017



The Chevin Technology XGMAC IP core provides high performance, Ultra low-latency 10Gbit/s Ethernet connectivity in Xilinx FPGAs. The XGMAC user guide and reference design simplifies the FPGA integration process, and can be used directly with an external or internal PCS. We recommend using Chevin Technology's XGPCS to achieve the lowest possible latency.

The application side can be driven by any logic that generates and decodes Ethernet frames. The XGMAC manages frame timing, CRC32 Checksum insertion and generation, and manages the lower layer fault handling and XGMII interface coding. Flow control provides back pressure to peer node and is handled automatically by the XGMAC in both directions independently. A detailed statistics block provides a running count of frames sent and received with individual 64bit counters for different frame sizes, types and checksum errors.

Achieve smoother, faster integration with the Chevin Technology reference design on an AlphaData boards; ADMPCIE KU3, ADM-PCIE-8V3, ADM-PCIE-9V3, or a Xilinx KC705 development board, and a simple "ping" command line with the ICMP/ARP options. Use standard software TCP/UDP tools when integrated with Chevin Technology's XGTCP IP core.

Key Features

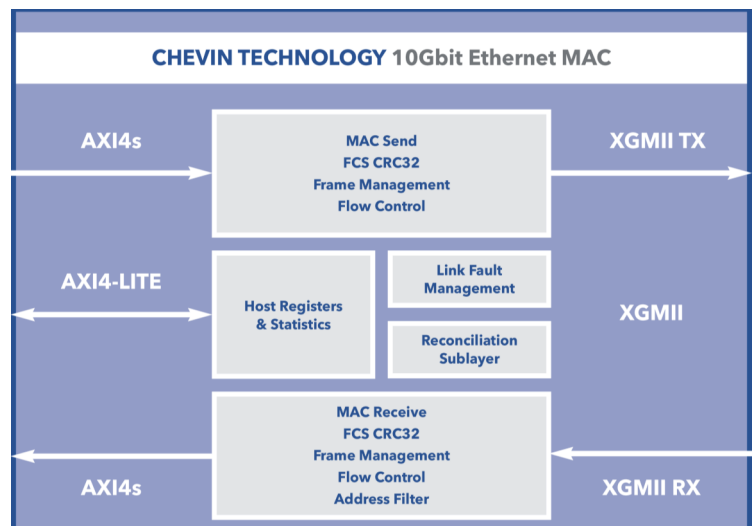
- Designed to IEEE 802.3-2008 Specification
- Low Latency 44.8 ns
- Integrated FCS CRC32 check/generate
- Small Footprint, 2749 LUTs
- Flow Control option with Pause packets
- Programmable max frame length
- Reconciliation Layer -Local /Remote Faults
- Programmable Inter Frame Gap
- Deficit Idle Count for maximum throughput
- Cut-through mode for lowest latency
- Store-and-forward for minimum app load
- MAC address filtering options
- Detailed traffic analysis statistics collection
- Optional MDIO master for controlling PHY

Latency Figures

First byte App IF to first byte XGMII	25.6ns
First byte XGMII to first byte App IF	19.2ns
Full Round trip time, including MAC/PCS/PMA AppTX -> SFP+ (wire) -> AppRX	160 ns

FPGA Resource Figures

XGMAC - Cut-through	2749 LUTs
XGMAC (Store&Fwd, with stats)	2900 LUTs
Options: Store & Forward	4 BRAMs



Deliverables

- Encrypted RTL/VHDL source code for simulation
- Encrypted compiled netlist
- Datasheet & User Guide to assist integration
- Reference Designs for Alpha-Data boards
ADM-PCIE-KU3, ADM-PCIE-8V3, ADM-PCIE-9V3
- Simulation Test bench
- Build scripts for Vivado
- Support for integration into FPGA



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10Gbit/s Ethernet MAC

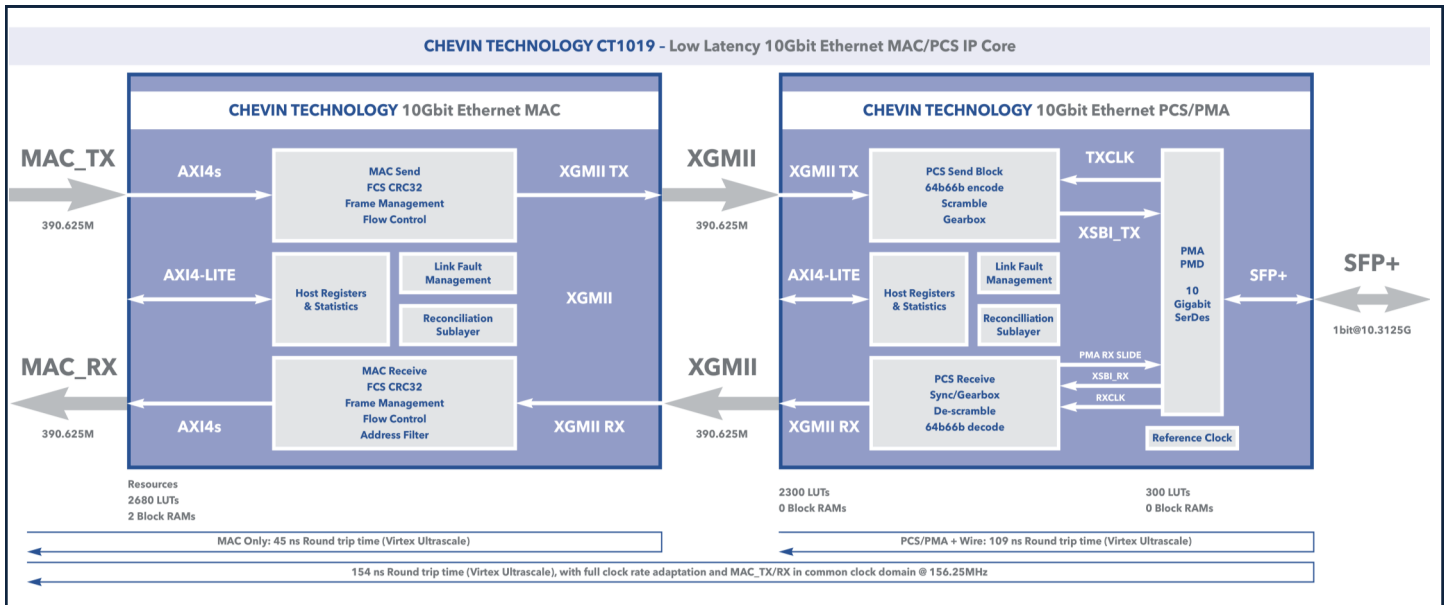
XGMAC - Integration in FPGA

A simple host interface allows control and configuration of the XGMAC registers and statistics block. The reference design includes a UART host interface port and example host software to drive this interface and can be used to speed up integration work.

The 64bit XGMII interface connects directly to any XGMII compatible PHY preferably utilizing Kintex, Virtex and UltraScale devices' 10Gbit capable SerDes (Multi Gigabit Transceivers) that provide the lowest latency, power, board size and cost, and the best overall performance.

We recommend pairing the XGMAC with Chevin Technology's XGPCS, an ultra-low-latency 10GBASE-R block for SFP+ Direct Attach copper cable or SR/LR Fiber connection.

The application side connects directly to user logic which can be user logic FIFOs to AXI4 standard interfaces or shared via an arbiter to other stack layers such as TCP/IP, UDP/IP, ICMP and ARP, also supplied by Chevin Technology, for a more integrated FPGA solution.



Chevin Technology IP



10G PCS/PMA

10G LL MAC & PCS/PMA



25G MAC

25G PCS/PMA

25G LLMAC & PCS/PMA



SATAv3.2 – 1.5/3/6Gbit/s SSD Host Ctrl



25G UDP
25G TCP

XGTCP - 10Gbit/s TCP Server/Client
XGUDP - 10Gbit/s UDP Server/Client
XGICMP/ARP – 10Gbit/s support library
XGUDT4 – 10Gbit/s UDT4 Server

Markets

- Finance
- Telecoms
- Broadcast
- Defense/ Government
- Oil and Gas

Applications

- Trade execution & monitoring
- Data Storage & Capture systems
- HPC / Big Data systems
- Signal processing systems
- Data Mining

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