25Gbit/s LL Ethernet MAC/PCS

Ultra Low-Latency Ethernet IP for FPGAs

CT1029-25GbE-LL-MAC/PCS
Product Brief - Version 1.1 – 5th July 2017

The Chevin Technology **25G LL MAC/PCS** combines the **25G MAC** and **25G PCS** IP cores to obtain the lowest possible latency while simplifying the integration of 25Gbit/s Ethernet connectivity in Xilinx Virtex® UltraScale™ FPGAs.

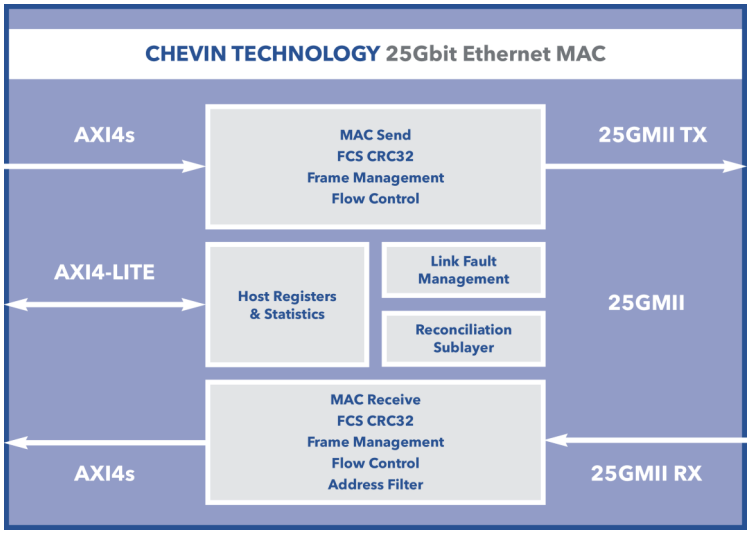
Ultra-low latency is achieved on the PCS block by using only the PMA function in FPGA Multi-Gigabit transceivers and moving all PCS functions to code that is optimized for 25GBASE-R. This allows the data to take the shortest, therefore the lowest, latency path to and from the wire.

The MAC manages frame timing, CRC32 Checksum insertion and generation, and manages the lower layer fault handling and 25GMII interface coding. Chevin Technology's MAC/PCS is 25GMII compatible with a 64bit interface at 390.625MHz. A detailed statistics block provides a running count of frames sent and received with individual 64bit counters for different frame sizes, types and checksum errors.

Achieve smoother, faster integration with the Chevin Technology reference design on AlphaData boards; ADM-PCIE-8V3, ADM-PCIE-9V3, Xilinx Virtex® UltraScale™ and UltraScale+™development boards.
Use standard software TCP/UDP tools when integrated with Chevin Technology's XGTCP or XGUDP IP cores.

Key Features

- Designed to IEEE 802.3by 25GBASE-R
- Ultra Low Latency 128 ns packet Round Trip Time (RTT) in Virtex® UltraScale™
- Integrated FCS CRC32 check/generate
- 7930 LUTs (MAC 2680 & PCS 5250LUTs)
- Flow Control option with Pause packets
- Deficit Idle Count / Programmable IFG– Minimize IFG
- Cut-through mode for minimum latency
- Store-and-forward for minimum app load
- Fault Management, BER monitoring
- Statistics counters for frames and bytes sent/ received, size bins, FCS errors, broadcast



Deliverables

- Encrypted RTL/VHDL source code for simulation
- Encrypted compiled netlist
- Datasheet & User Guide to assist integration
- Reference Designs for Alpha-Data boards ADM-PCIE-8V3, ADM-PCIE-9V3
- Simulation Test bench
- Build scripts for Vivado
- Support for integration into FPGA

Latency Figures

Round trip delay (Ultrascale)

MAC(in) -> SFP28 (wire) -> MAC(out)	128ns

FPGA Resource Figures

Device: Virtex® UltraScale™ xcvu095 -2

25GPCS/PMA	5250 LUTs
25GMAC	2680 LUTs
Options:	
Store & Forward	4 BRAMs

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25G LL MAC/PCS

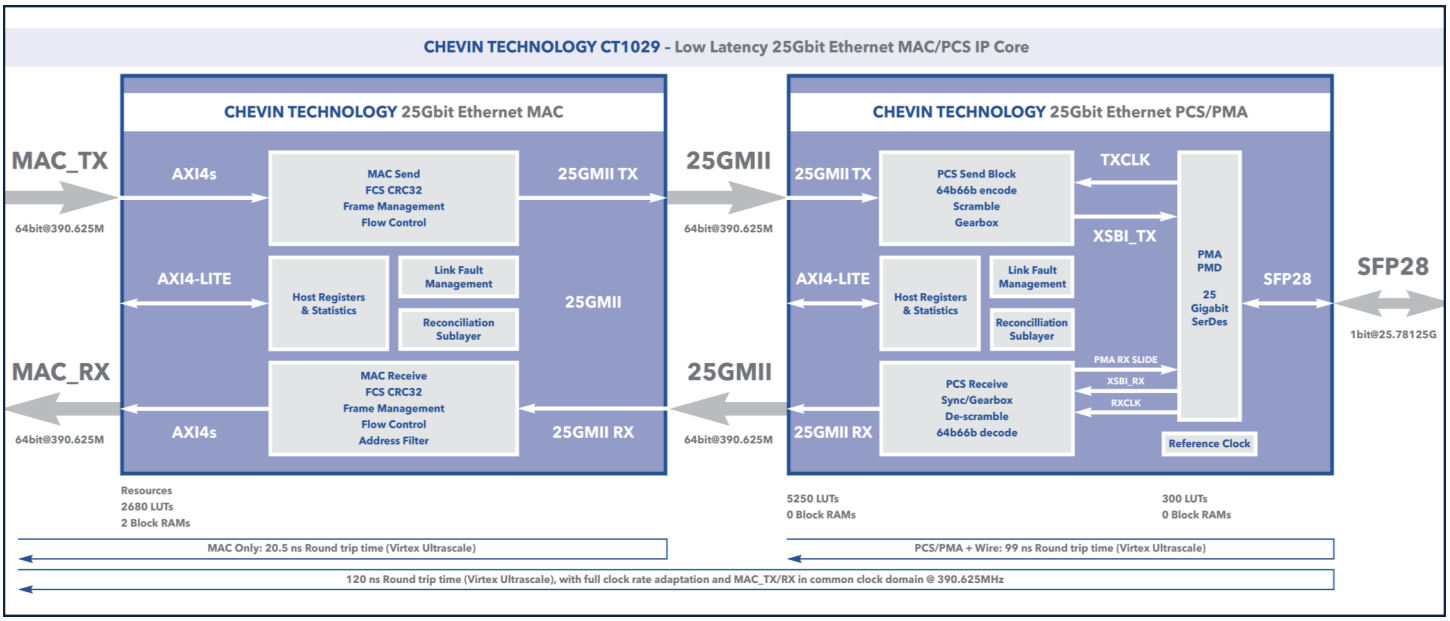
Integration in FPGA

The reference design includes a top level wrapper for the IP and includes build scripts and constraints.

A simple host interface makes it possible to read and write registers for monitoring purposes, and can be used to speed up integration work.

The 64bit 25GMII interface connects directly to any 25GMII compatible PCS, preferably utilizing Virtex® UltraScale™ devices that are 25Gbit capable. This combination provides the lowest possible latency, power, board size and cost, and the best overall performance.

The application side connects directly to user logic which can be user logic FIFOs to AXI4 standard interfaces or shared via an arbiter to other stack layers such as TCP/IP, UDP/IP, ICMP and ARP, also supplied by Chevin Technology, for a more integrated FPGA solution.



Chevin Technology IP

10G Ethernet

10G PCS/PMA

10G LL MAC & PCS/PMA

10G MAC

SSD STORAGE

SATAv3.2 – 1.5/3/6Gbit/s SSD Host Ctrl

25G Ethernet

25G MAC

25G PCS/PMA

25G LLMAC & PCS/PMA

ETHERNET PROTOCOLS

25G UDP, 25G TCP
XGTCP - 10Gbit/s TCP Server/Client
XGUDP - 10Gbit/s UDP Server/Client
XGICMP/ARP – 10Gbit/s support library
XGUDT4 – 10Gbit/s UDT4 Server

Markets

- Finance
- Telecoms
- Broadcast
- Defense/ Government
- Oil and Gas

Applications

- Trade execution & monitoring
- Data Storage & Capture systems
- HPC / Big Data systems
- Signal processing systems
- Data Mining

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