

TCP/ Internet Protocol for 10 & 25 Gbit/s Ethernet

CT1008-XGUDP - Product Brief - Version 1.0 – 31st October 2017



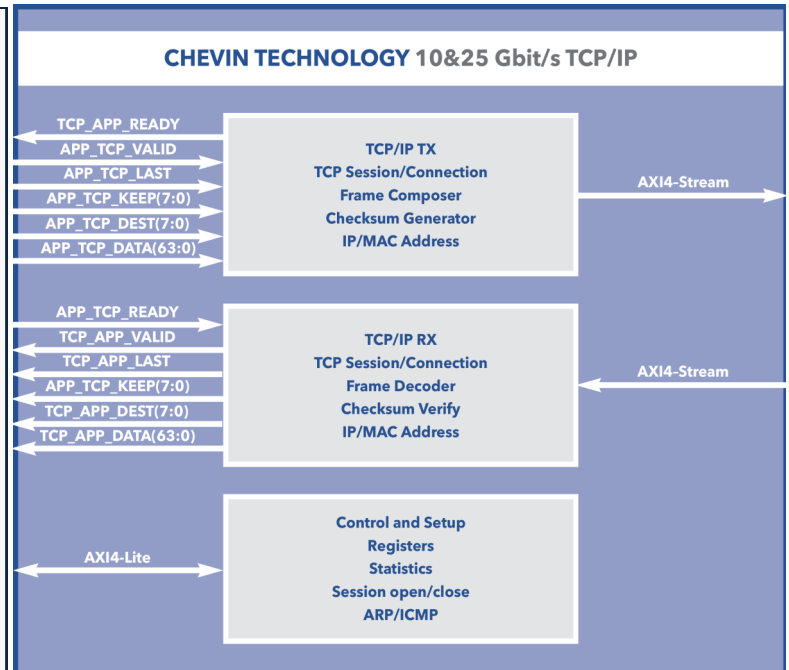
Chevin Technology's TCP/IP Offload Engine is an FPGA Synthesisable Ethernet TCP/IP server/client in a lean and fast, all-RTL solution. The TCP/IP can be used with both 10G & 25G Ethernet IP cores for reliable, low-latency connectivity in any FPGA using a minimum of resources. Chevin Technology's TCP/IP offloads the TCP protocol using fast and efficient logic for checksum calculation, and is easily integrated alongside other protocols to provide an easy path for the development of TCP enabled FPGA applications.

Chevin Technology's range of IP cores have been developed in house, so we can offer our customers expert advice and support, along with consistent, high performance Ethernet connectivity. Chevin Technology offer a complete IP stack including 10&25G PCS/PMA (physical layer), 10&25G MAC (link layer), and TCP or UDP (network and transport layer).

Reference designs are available on selected boards using standard software development tools when integrated with higher layers from Chevin Technology's range of IP blocks.

Key Features

- 1 to 256 simultaneous TCP/IP connections
- Server/Client roles, configurable per connection
- Hash table based filtering for minimum latency
- Low-jitter sustained high throughput performance
- Programmable per connection receive/congestion window
- Monitoring function; 'bump-in-the-wire' inspection, non-intrusive packet analysis
- Cut-through mode for absolute highest throughput and lowest latency
- Store-and-Forward mode ensures ultimate safety in verified data to and from the application.
- Configurable TX & RX buffer size: 1KB-1GB
- 64-bit AXI4 stream @ 156.25 MHz



Deliverables

- Encrypted compiled netlist
- Datasheet & User Guide to assist integration
- Reference Designs for Xilinx KC705 board & AlphaData boards ADM-PCIE-KU3, ADM-PCIE-8V3, ADM-PCIE-9V3,
- Simulation Test bench
- Build scripts for Vivado
- Support for integration into FPGA

FPGA Resource Figures

Devices: Xilinx Virtex UltraScale; Kintex Ultrascale; Kintex-7; Zynq

Small Memory Footprint 25 BRAMs + packet buffer; 12000 LUTs for 16 sessions

Options: External DDR3 packet buffer;

+ ARP/ICMP 1100 LUTS



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TCP/IP for 10 & 25Gbit/s Ethernet

TCP/IP - Integration in FPGA

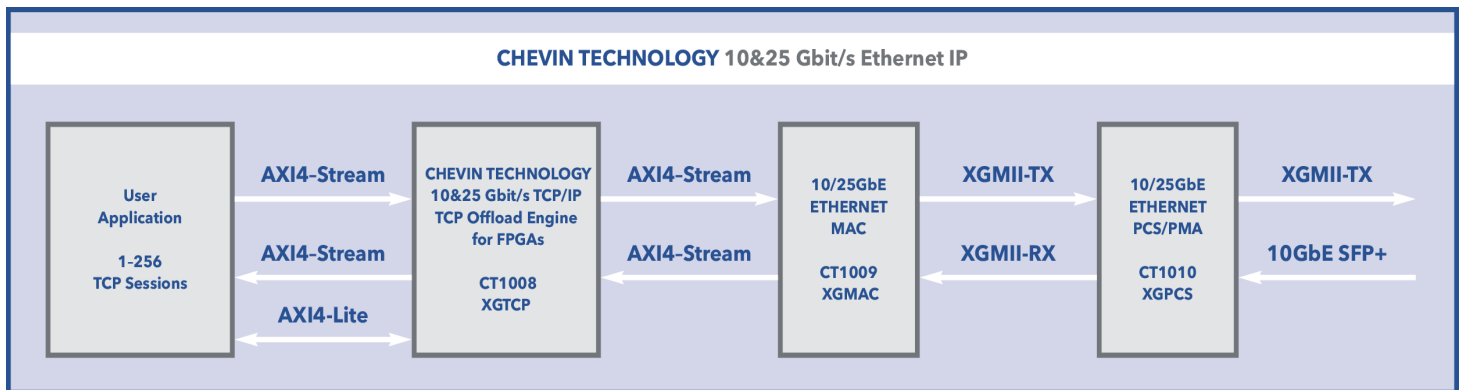


The TCP/IP Offload Engine provides a quick path to creating TCP enabled applications with a minimum of additional resources for network management at the FPGA side.

The AXI4-Lite host interface permits control and configuration of the TCP/IP blocks' registers and statistics for connection and link monitoring. The User application side and MAC connect to the TCP/IP with an easy to use AXI4-Stream interface. The TCP/IP can be configured to initiate (client) or accept (server) a TCP connection with a remote endpoint. Once a session is established, the TCP /IP can send and receive data reliably over the TCP protocol; taking care of checksum insertion/checking, sockets and flow control all at high, sustained data rates of 10 or 25 Gbit/s.

The User interface provides flow control, and manages multiple connections. Multiple simultaneous connections are supported, limited only by available packet buffer resources. Opening and closing connections is handled by the TCP block, with no requirement for additional software support. Re-transmit is handled by a control layer within the TCP for fast, easy error recovery.

Statistics are collected for all sent and received frames for traffic and connection analysis .



Chevin Technology IP



10G PCS/PMA
10G LL MAC & PCS/PMA



SATAv3.2 – 1.5/3/6Gbit/s SSD Host Ctrl



25G MAC
25G PCS/PMA
25G LLMAC & PCS/PMA



25G TCP
XGTCP - 10Gbit/s TCP Server/Client
XGICMP/ARP – 10Gbit/s support library
XGUDT4 – 10Gbit/s UDT4 Server

Markets

- Finance
- Telecoms
- Broadcast
- Defense/ Government
- Oil and Gas

Applications

- Trade execution & monitoring
- Data Storage & Capture systems
- HPC / Big Data systems
- Signal processing systems
- Data Mining
- Artificial Intelligence

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