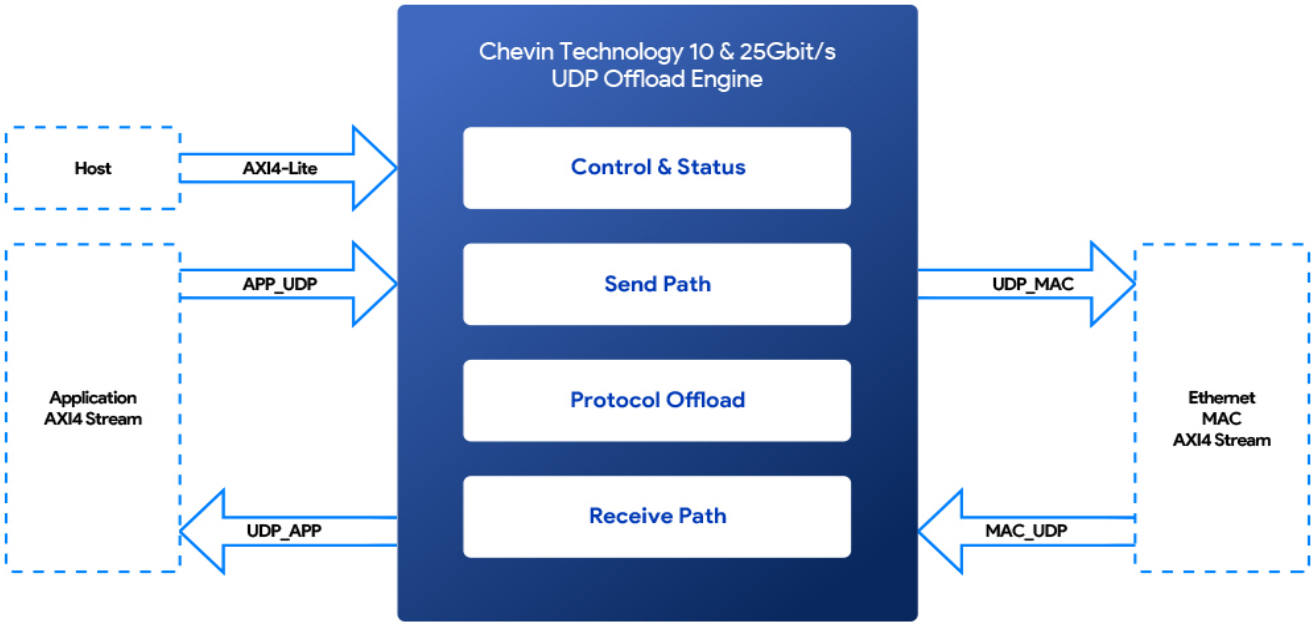
10G/25G UDP/IP Offload Engine

CT1012-UDP/IP - Product Brief - Version 2.1– February 2023

User Datagram Protocol (UDP/IP) is a communications protocol used for establishing connections between applications on the Internet. The UDP is a transport layer that runs on top of the Internet Protocol (IP) Layer. Chevin Technology's 10G & 25G UDP Ethernet IP core is an FPGA Synthesisable Offload Engine with Checksum Offload for ultra low-latency connectivity. The UDP/IP is configurable for Intel and Xilinx FPGAs, and simplifies integration by handling the complete Ethernet frame assembly. Chevin Technology's UDP/IP is a mature IP core with proven success in customers' projects. A simple AXI4 streaming interface is all that is required to start sending and receiving UDP datagrams, and only the user data payload is exchanged between the application and the UDP block. For a single port application the port number can be set to a constant, hard coded or software configurable. A multi- port application is supported by a single UDP/ IP core by using the TDEST sideband embedded in the streaming interface.



Deliverables

- *Encrypted compiled netlist*
- *Datasheet & User Guide*
- *Reference Designs*
- *Simulation Test bench*
- *Build scripts for Vivado, Quartus*
- *Support for integration into FPGA*

Key Features

- *AXI4s MAC & Application Interfaces*
- *Designed to UDP specification RFC 768*
- *Compose/Decompose complete UDP Datagrams*
- *IP frame Checksum Generator/Checker*
- *Jumbo frame support up to 32kbyte*
- *Configurable operation port filtering*
- *1-64k Ports (configurable ports & filters)*
- *Detailed traffic analysis statistics collection*
- *Integrated Streaming FIFO – 4 Block RAMs*
- *Flow Control between MAC/User logic*

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10G/25G

UDP/IP Offload Engine

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Chevin Technology's UDP IP core offloads frame assembly with hardware accelerated checksum calculation for UDP datagrams. The application side FIFO provides independent TX/RX buffering and flow control between Application logic and UDP, over a streaming 64bit interface in a single clock domain. Remote port information is multiplexed with the streaming interface to provide a flexible solution for application logic.

A detailed statistics block provides a running count of frames sent and received , number of bytes sent/received, frames dropped due to flow control, last sent/received frame size and optional timestamp. Reference designs are available on selected boards using standard software development tools. The application side can connect directly to any 64bit MAC with an easy to use streaming AXI4s interface.

We recommend pairing the UDP/IP with Chevin Technology's MAC, an ultra-low-latency Ethernet MAC and other stack layers such as ICMP and ARP, for a more integrated FPGA solution.

Throughput & Latency Figures

UDP send/receive rate: 10 Gbps (1.25GB/s), TX 38.4 ns, RX 38.4 ns

Round trip delay MAC -> APP -> MAC 102.4ns

(Figures above include 33.6ns of inherent protocol latency)

FPGA Devices/ Resource Figures

Intel: Agilex, Stratix, Arria

Xilinx: Virtex UltraScale: 2480 LUTs, Kintex Ultrascale: 2480 LUTs , Kintex-7: 3088 LUTs

Small Memory Footprint 14 RAMs

Options: + ARP/ICMP 920 LUTS

Markets

- *Defence*
- *Scientific*
- *Aerospace*
- *Cyber security*
- *Medical*
- *Finance*
- *Telecoms*
- *Broadcast*
- *Data Centre*

Applications

- *Artificial Intelligence*
- *Machine Learning*
- *Video Imaging*
- *Image/Signal Processing*
- *Internet Security Monitoring*
- *Data Storage & Capture Systems*
- *Trade Execution & monitoring*
- *HPC/ Big Data systems*
- *Data Mining*

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